WHAT IS CLAIMED IS:

1. A microprocessor, comprising:

a dispatch unit configured to dispatch operations;

a scheduler coupled to the dispatch unit and configured to schedule dispatched operations for execution;

wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction.

2. The microprocessor of claim 1, wherein the dispatch unit is further configured to dispatch an operation that provides one or more register names for use as replacement register names within the microcode subroutine.

3. The microprocessor of claim 2, wherein the dispatch unit is configured to allocate an alias table element to store the one or more register names in response to handling the operation.

4. The microprocessor of claim 2, wherein the dispatch unit is configured to maintain multiple allocated alias table elements at a same time.

5. The microprocessor of claim 4, wherein each of the multiple allocated alias table elements is associated with a respective microcode subroutine, wherein the dispatch unit is configured to maintain each alias table element at least until all branch operations within the respective microcode subroutine have resolved.

6. The microprocessor of claim 4, wherein in response to detection of a branch misprediction within a microcode subroutine, the dispatch unit is configured to perform replacements within one or more microcode operations included within the microcode subroutine according to the one or more register names stored within a respective alias table element and to dispatch the one or more microcode operations subsequent to performing the replacements.

7. The microprocessor of claim 2, further comprising a trace cache coupled to the dispatch unit, wherein the trace cache includes a trace cache entry; wherein a trace stored in the trace cache entry includes the microcode subroutine call operation and the one or more register names for use as replacement register names.

8. The microprocessor of claim 7, wherein in response to receiving the trace from the trace cache, the dispatch unit is configured to allocate an alias table to store the one or more register names.

9. The microprocessor of claim 1, wherein the dispatch unit is configured to store the microcode subroutine in one or more microcode traces.

10. The microprocessor of claim 9, wherein the one or more microcode traces are stored within a read only memory.

11. The microprocessor of claim 9, wherein each microcode operation stored in the one or more microcode traces includes an associated liveness indication.

12. The microprocessor of claim 11, wherein the dispatch unit is configured to determine whether each microcode operation stored in one of the one or more microcode traces is executable dependent on at least one of: a branch prediction and the associated liveness indication;

wherein the dispatch unit is configured to signal whether each microcode operation stored in the one of the one or more microcode traces is executable when dispatching that microcode operation to the scheduler;

wherein the scheduler is configured to store an associated indication for each dispatched microcode operation indicating whether that dispatched microcode operation is executable.

13. The microprocessor of claim 12, wherein if the branch prediction is incorrect, the scheduler is configured to update the associated indication for at least one dispatched microcode operation.

14. The microprocessor of claim 11, wherein the dispatch unit is configured to selectively dispatch microcode operations included in the one or more microcode traces dependent upon at least one of: the associated liveness indication and a branch prediction.

15. The microprocessor of claim 1, wherein a same opcode is used to specify the microcode subroutine call operation and a non-microcode subroutine call operation.

16. The microprocessor of claim 1, wherein the microcode subroutine includes a return operation, wherein the return operation pops a return address from a stack, wherein execution of the microcode subroutine call operation pushes the return address onto the stack.

17. A computer system, comprising:

a system memory; and

a microprocessor coupled to the system memory, wherein the microprocessor comprises:

a dispatch unit configured to dispatch operations;

a scheduler coupled to the dispatch unit and configured to schedule dispatched operations for execution;

wherein in response to receiving a microcoded instruction, the dispatch unit is configured to dispatch to the scheduler a microcode subroutine call operation that includes a tag identifying a microcode subroutine associated with the microcoded instruction.

18. The computer system of claim 17, wherein the dispatch unit is further configured to dispatch an operation that provides one or more register names for use as replacement register names within the microcode subroutine.

19. The computer system of claim 18, wherein the dispatch unit is configured to allocate an alias table element to store the one or more register names in response to handling the operation.

20. The computer system of claim 18, wherein the dispatch unit is configured to maintain multiple allocated alias table elements at a same time.

21. The computer system of claim 20, wherein each of the multiple allocated alias table elements associated with a respective microcode subroutine, wherein the dispatch unit is configured to maintain each alias table element at least until all branch operations within the respective microcode subroutine have resolved.

22. The computer system of claim 20, wherein in response to detection of a branch misprediction within a microcode subroutine, the dispatch unit is configured to perform replacements within one or more microcode operations included within the microcode subroutine according to the one or more register names stored within a respective alias

table element and to dispatch the one or more microcode operations subsequent to performing the replacements.

23. The computer system of claim 18, further comprising a trace cache coupled to the dispatch unit, wherein the trace cache includes a trace cache entry; wherein a trace stored in the trace cache entry includes the microcode subroutine call operation and the one or more register names for use as replacement values.

24. The computer system of claim 23, wherein in response to receiving the trace from the trace cache, the dispatch unit is configured to allocate an alias table to store the one or more register names.

25. The computer system of claim 17, wherein the dispatch unit is configured to store the microcode subroutine in one or more microcode traces.

26. The computer system of claim 25, wherein each microcode operation stored in the one or more microcode traces includes an associated liveness indication.

27. The computer system of claim 17, wherein a same opcode is used to specify the microcode subroutine call operation and a non-microcode subroutine call operation.

28. The computer system of claim 17, wherein the microcode subroutine includes a return operation, wherein the return operation pops a return address from a stack, wherein execution of the microcode subroutine call operation pushes the return address onto the stack.

29. A method, comprising:

receiving a stream of instructions;

detecting a microcoded instruction within the stream of instructions, wherein the microcoded instruction immediately precedes an other instruction in program order;

in response to said detecting, dispatching a microcode subroutine call operation that identifies a microcode subroutine associated with the microcoded instruction, wherein the microcode subroutine call operation pushes an address of the other instruction onto a stack; and

executing a plurality of operations included in the microcode subroutine, wherein the plurality of operations include a return operation, and wherein execution of the return operation pops the address from the stack.

30. The method of claim 29, further comprising dispatching an operation that provides one or more register names for use as replacement register names within the microcode subroutine in response to said detecting.

31. The method of claim 30, further comprising allocating an alias table element to store the one or more register names in response to handling the operation that provides one or more register names for use as replacement register names.

32. The method of claim 31, further comprising replacing one or more register names within one or more microcode operations included in the microcode subroutine with the one or more register names from the alias table element in response to detection of a branch misprediction within the microcode subroutine.

33. The method of claim 30, further comprising maintaining multiple allocated alias table elements at a same time, wherein each of the multiple allocated alias table elements is associated with a different microcode subroutine.

34. The method of claim 33, wherein said maintaining comprises maintaining each alias table element at least until resolution of all branch operations within a respective microcode subroutine.

35. The method of claim 30, further comprising storing the microcode subroutine call operation and the one or more register names for use as replacement register names within a trace.

36. The method of claim 35, further comprising allocating an alias table element to store the one or more register names in response to fetching the trace from the trace cache.

37. The method of claim 1, further comprising storing the microcode subroutine in one or more microcode traces.

38. The method of claim 37, further comprising storing a liveness indication for each microcode operation stored in the one or more microcode traces.

39. The method of claim 29, further comprising dispatching a non-microcode subroutine call operation, wherein a same opcode is used to specify the microcode subroutine call operation and the non-microcode subroutine call operation.

40. A method, comprising:

dispatching one or more operations included in a first microcode subroutine and one or more operations included in a second microcode subroutine, wherein said dispatching the one or more operations in the first microcode subroutine comprises performing register name replacements using replacement register names stored in a first alias table element and wherein said dispatching the one or more operations in the second

microcode subroutine comprises performing register name replacements using replacement register names stored in a second alias table element;

subsequent to said dispatching, detecting a branch misprediction within the first microcode subroutine;

in response to said detecting, replacing register names within one or more other operations included in the first microcode subroutine with replacement register names stored in the first alias table element; and

dispatching the one or more other operations subsequent to said replacing.

41. A system, comprising:

means for receiving a stream of instructions, decoding each non-microcoded instruction within the stream of instructions into one or more operations, and dispatching each of the one or more operations;

means for executing dispatched operations;

wherein the means for receiving the stream of instructions are configured to detect a microcoded instruction within the stream of instructions and to responsively dispatch a microcode subroutine call operation that identifies a microcode subroutine associated with the microcoded instruction;

wherein the means for executing dispatched operations are configured to push an address onto a stack when executing the microcode subroutine call operation, wherein the address identifies an operation generated by decoding a non-microcoded instruction immediately subsequent to the microcoded instruction within the stream of instructions.